SPICEVISION® PRO

concept engineering

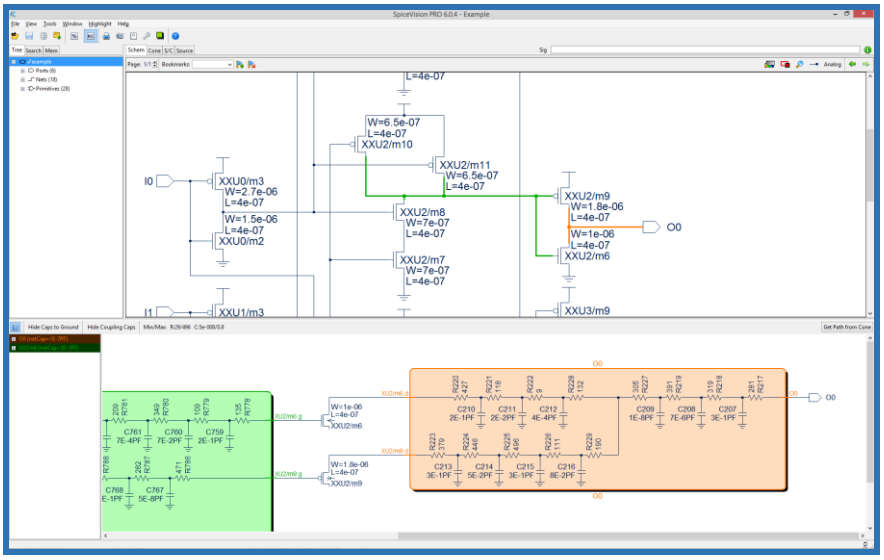
SpiceVision® PRO: A Customizable Transistor-Level Debugger and SPICE Netlist Viewer

SpiceVision PRO takes any SPICE netlist, SPICE model and extracted parasitic netlist and generates clean, easy-to-read transistor-level schematics, and design documentation to speed up circuit desgin, circuit debugging, and circuit optimization at the transistor-level.

Simplification – SpiceVision PRO can simplify the displayed schematics, merging components in parallel, such as transistors, or creating a non-parasitic view, showing only functionality.

Automatic Logic Recognition – The built-in automatic logic recognition engine creates digital logic schematics from pure CMOS SPICE-level netlists for easy design exploration.

Customization – Users can write API code (Tcl programming language) to analyze the design data and to generate user-specific design reports and electrical design rule checks (ERC).



- Netlist analyzer for SPICE, HSPICE®, Spectre®, Eldo®, CDL, Calibre®, SPEF and DSPF
- Automatic Logic Recognition – reads SPICE and shows logic functions
- Tcl based UserWare API – for advanced customization and ERC
- 64-bit database handles today's largest SoCs and ASICs
- Schematic export to Cadence Virtuoso® (option)
- Easy Navigation – Cone Window displays selected fragments and critical paths
- Cookie-cutting – circuit fragments can be isolated and saved as SPICE netlists

Assistance for fast SPICE Simulation – The Cone Window, an "intelligent magnifying glass", displays selected circuit fragments, including critical paths. These circuit fragments can be transferred to a simulator as separate SPICE netlist files, for partial simulation, often running 10 to 100 times faster than a full simulation.

Post-Layout Debugging – Layout extraction tools generate very large and complex SPEF or DSPF netlists with many critical path elements. These paths can be extracted, displayed, and saved for fast and detailed critical path simulation (parasitic analysis option).

IP Reuse / SPICE Netlist Export – Specific parts of a SPICE netlist can be cookie-cut from the complete design, for example from a large flat SPICE netlist, and saved as a new small SPICE netlist file for critical path simulation or as a schematic diagram (schematic export option), for use as new IP building block.

Cadence Interface / Netlist to Schematic – The Virtuoso® Schematic Export option, based on the Cadence SKILL® language, exports schematics and schematic fragments into the Cadence Virtuoso® Schematic Editor environment.

Fast SPICE Viewer – SPICE files are difficult to read and understand. Within seconds SpiceVision PRO gives engineers an extra level of understanding of the circuits that are defined in their SPICE netlist files. It is easier to debug and optimize designs and devices can move into production earlier and with a higher degree of confidence.

At a Glance

FEATURE	BENEFITS
Schematics from SPICE netlists	Schematics provide easier and faster debugging for complex circuits. Supported dialects include SPICE, HSPICE®, Spectre®, Calibre®, CDL, Eldo® and PSPICE®.
Automatic logic recognition	The built-in automatic logic recognition engine creates digital logic schematics from pure CMOS SPICE-level netlists for easy design exploration
Ultra fast SPICE-reader	SPICE to schematics on the fly (within seconds)
Fragment save	Fragments of a circuit can be saved as SPICE netlist files and schematics for future reuse as IP building block, or for partial simulation
64-bit database	Higher performance and increased capacity, for very large designs
Powerful GUI	Multiple views, including tree, schematic, cone and source file for increased circuit understanding plus drag-and-drop between different views
Cone Window	Incremental schematic navigation for big designs
Tcl UserWare API	Allows interfacing with tool flow and definition of electrical rule checks
Schematic export option Cadence interface	Export schematics and schematic fragments into Cadence Virtuoso® Schematic Editor for optimization, debugging and IP reuse
Parasitic analysis option	Allows visualization and analysis of parasitic networks (SPEF and DSPF netlists) and provides capabilities to create SPICE netlists for critical path simulation

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