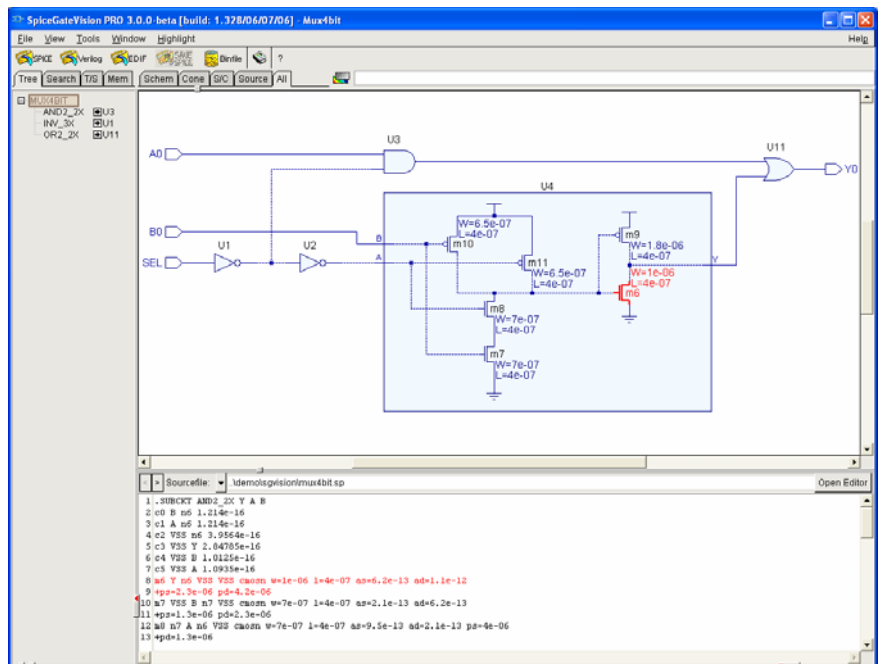


SGvision™ PRO: Mixed-mode debugging in a single tool

SGvision™ PRO is a new tool to analyze mixed level descriptions, both top level structures described in Verilog and lower level structures described via SPICE, can be debugged in a single integrated environment.

To optimize or debug a device a designer may choose to work at transistor-level for critical areas such as IP/Library components and analog blocks, while staying at gate-level for other areas of the design. Debugging such a design has previously required separate tools: with SGvision PRO, it is now possible to see the schematics and traverse the signal flow of both the gates and the transistors in the same window, improving understanding of the circuits and accelerating analysis and debugging.



- Mixed mode graphical analyzer – Verilog and SPICE in a single tool
- As detailed as you want – Debugging at gate-level and transistor-level
- Logic cone – debug selected fragments or critical paths
- 32/64 bit database – handles the largest SoCs and ASICs
- Tcl based UserWare API – for advanced customization
- Cookie cutting – circuit fragments can be saved as separate SPICE files

Tcl based API – the Tcl Based UserWare API provides very flexible customization options, allowing SGvision PRO to match individual needs, corporate standards or to be integrated into an organizations design flow.

Customer driven – users of the existing Concept Engineering debugging tools, GateVision® PRO for gate-level and SpiceVision® PRO for transistor-level, have asked for a single interface for mixed level debugging. SGvision PRO provides just this tool, combining two tools in one for flexibility and power in debugging.

32/64 bit – SGvision PRO runs on powerful 64 bit platforms, such as XEON®, Opteron™, UltraSPARC®, Itanium® and POWER™. The underlying database, specially developed for 32/64 bit operation, allows even the most complex of today's SoC and ASIC designs to be examined.

Circuit fragment debugging – the Logic Cone Window is an intelligent magnifying glass, allowing the engineer to concentrate on a specific circuit fragment or critical path, showing both gate- and transistor-level details in a single window. There is no distraction from irrelevant graphics and information, yet there are links to the source code, whether Verilog or SPICE. The fragment under investigation can be independently exported as a SPICE netlist and can be used for the fast simulation of critical circuit fragments. It is not necessary to simulate the whole design, reducing simulation and development time drastically.

Improved productivity – being able to analyze both gate-level and transistor-level at the same time in just one debug cockpit increases design and verification engineers productivity, reducing product development and debug cycle time.

At a Glance

FEATURE	BENEFITS
Support for Verilog, EDIF and SPICE dialects in a single tool	Engineers can quickly and easily understand and debug mixed-mode designs
Interactive graphic fragment navigation	Reduces debug complexity and increases engineering productivity
Object cross-probing	By highlighting objects in all design views (schematic, logic cone and source code), helps shorten design and debug time
Tcl UserWare API	Allows user customization and interfacing to the design tool flow
32/64 bit platform support	Power to cope with the largest mixed-mode SoCs and ASICs
Non-Parasitic view	Displays CMOS function without parasitic structures for comprehension of circuit
Predefined symbols	Standard symbols for transistors, resistors capacitors etc, supplied. Can link to external symbol library to meet local conventions
Fragment save	Fragments of circuits can be saved as SPICE file and schematic for future reuse as IP, or for partial simulation
Parasitic analysis option	Allows visualization and analysis of parasitic networks (DSPF) and provides capabilities to create SPICE netlists for critical parasitic network fragments

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