

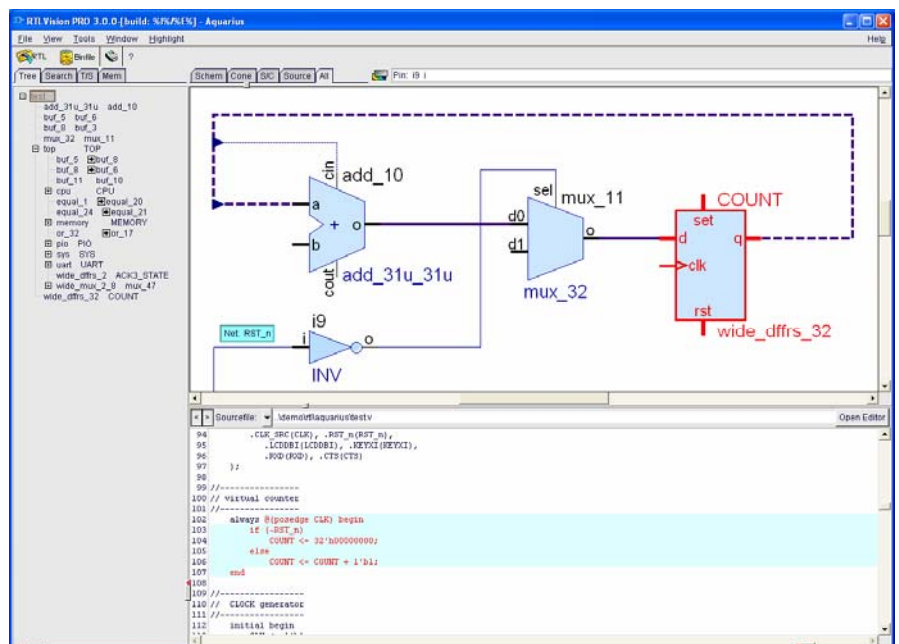


RTLvision® PRO: Understand and Debug High Level Designs, Easily

It is no longer possible to carry out all ASIC and SoC designs from scratch; elements of previous designs have to be re-used and third party IP blocks are embedded very often. But understanding the RTL for third party IP or legacy code is not always easy, making it time consuming and difficult to modify and integrate into the new design.

RTLvision® PRO provides fast visualization of RTL, so that engineers can easily understand, and implement existing code elements, whether in VHDL, Verilog or System Verilog.

Clock Tree Extraction – Clock signals are very often a source of problems when integrating separate code elements; RTLvision PRO can automatically extract and analyze clock trees and clock domains, giving an immediate view of the issues involved.



- Understand high-level designs – fast visualization makes legacy code, IP code etc easier to understand, debug, modify and integrate
- Mixed language capability – support for System Verilog, Verilog and VHDL matches the demands of today's complex heterogeneous designs
- Interactive fragment navigation – Logic Cone Window displays a visualization of just critical sections of RTL linked to original source code
- Tcl based UserWare API – access to database and GUI for project-specific or company-specific customization
- Ultra fast RTL readers and intuitive GUI – for ease of use

Fast Reader and Fragment Viewing – The RTLvision PRO can read HDL and display the underlying circuits on the fly, providing the engineer with immediate understanding of functionality of the RTL description. To accelerate debugging, critical code portions can be graphically displayed in the Logic Cone Window. An engineer can concentrate on that critical fragment, with links to the original source code, while not bothering about other areas of the design.

Incremental compilation – RTLvision PRO can visualize VHDL, Verilog and System Verilog code, matching the needs of today's most complex heterogeneous designs. It also supports incremental compilation, re-compiling only those areas that are affected by change, further reducing development time.

Documentation – The automated documentation feature of RTLvision PRO provides detailed design documentation of new, changed and re-used code, all to the same standard.

Customization – To meet the needs of a specific project or an organization's own standards a tcl based UserWare API allows the functionality of RTLvision PRO to be extended and tailored. Customers can use this API to easily perform company specific Electrical Rule Checks (ERC).

At a Glance

FEATURE	BENEFITS
Ultra fast HDL reader and graphics on the fly	Graphical representations make it easier to understand, debug, change and implement RTL code
Interactive Graphic Fragment Navigation shows only critical fragments of the RTL	Being able to identify and concentrate on a fragment helps to reduce complexity of the debug process and makes it easier to understand and change RTL code
Automatic clock trees and clock domains extraction and visualization	Faster detection and resolution of clock domain problems
Full support for mixed language designs (SystemVerilog, Verilog, VHDL)	Designers can easily develop and debug today's most complex heterogeneous designs
Incremental design compilation	Design updates can be faster, with only changed areas re-compiled
Automated design documentation	New and re-used code can be documented automatically
Tcl API	RTLvision PRO can be interfaced with the tool flow and the user can extend functionality to match project needs

Company Contact

Concept Engineering GmbH · Bötzingen Str. 29 · 79111 Freiburg · Germany
 Tel: +49-761- 47094-0 · Fax: +49-761- 47094-29 · Email: info@concept.de · http://www.concept.de