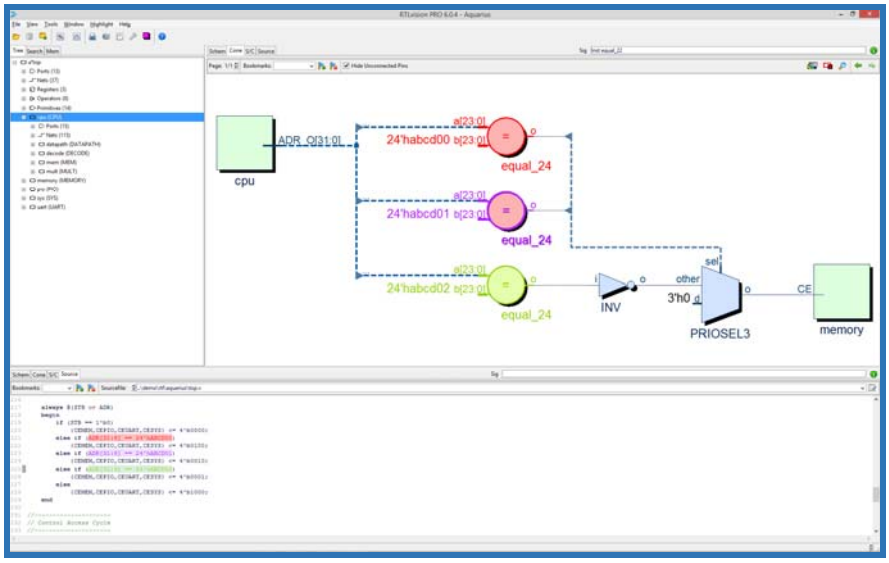
RTLVISION® PRO

concept engineering

RTLvision® PRO: Understand, Debug, and Integrate RTL Code, Easily

With rising chip complexity it is no longer possible to carry out SoC designs from scratch; RTL code of previous designs have to be re-used and third party IP blocks are often embedded. But understanding Verilog, VHDL or SystemVerilog code for third party IP or legacy RTL code is not always easy, making it time consuming and difficult to modify and integrate such code into the new design.



Fast RTL Viewer – RTLvision PRO provides fast visualization of RTL, so that engineers can easily understand and optimize code elements, whether in VHDL, Verilog or System Verilog.

Clock Tree Extraction – Clock signals are often a source of problems when integrating RTL code elements from different sources; RTLvision PRO automatically extracts and analyzes clock trees and gives an immediate view of the clock network and clock domains.

- RTL to schematics on the fly – fast RTL visualization makes RTL code elements and large designs easier to understand, debug, and modify
- Mixed language design – support for SystemVerilog, Verilog and VHDL matches the demands of today's complex SoC designs
- Integrated Waveform Viewer with source code link and schematic link
- Interactive fragment navigation – Logic Cone Window displays just the critical circuit sections and links to the RTL code
- Tcl based API for user-defined electrical rule checks and customization
- Ultra fast RTL readers and intuitive GUI – for ease of use
- VHDL viewer, Verilog viewer and SystemVerilog viewer in one tool
- Smart RTL Source Code Window – the interactive "Action Bar" within the RTL Source Code Window allows smart and context specific source code navigation.

Ultra Fast RTL Reader and Fragment Viewing – RTLvision PRO can read HDL and display the underlying circuits on the fly, providing the engineer with immediate understanding of functionality of the RTL description. To accelerate debugging, critical RTL code portions can be graphically displayed in the Logic Cone Window. An engineer can concentrate on that critical fragment, with links to the original RTL source code, while not bothering about other less important areas of the design.

Relaxed RTL Checking – Relaxed language checking allows improved handling of incomplete designs where IP building blocks are not yet properly defined.

Waveform Viewer and Signal Tracing – RTLvision PRO comes with a fully integrated waveform viewer and with support for interactive signal tracing in the source code, schematic view and waveform window. RTLvision PRO compiles VCD simulation data into its own high-speed format for accelerated waveform browsing and signal tracing.

Documentation – The automated documentation features of RTLvision PRO provide detailed design documentation of new, changed and re-used RTL code (schematics from Verilog code, schematics from VHDL code, PDF export, ...).

Customization – To meet the needs of a specific chip design project or an organization's own standards a Tcl based UserWare API allows the functionality of RTLvision PRO to be extended and tailored. Customers can use this API to easily perform company specific Electrical Rule Checks (ERC), and to interface RTLvision PRO with other tools.

At a Glance

FEATURE	BENEFITS
Fast RTL reader and schematics on the fly	Graphical representations make it easier to understand, debug, change and implement RTL code
Interactive Graphic Fragment Navigation shows only critical fragments of the RTL	Being able to identify and concentrate on a fragment makes it easier to understand and change RTL code
Automatic clock tree and clock domain extraction and visualization	Faster detection and resolution of clock domain problems
Integrated Waveform viewer	Waveform viewer supports interactive signal tracing
Full support for mixed language designs (SystemVerilog, Verilog, VHDL)	Designers can easily develop and debug today's most complex heterogeneous ASIC and SoC designs
RTL to schematics	Verilog viewer, VHDL viewer, and SystemVerilog viewer in one tool allows IP blocks from almost any source to be analyzed
Automated design documentation	New and re-used RTL code can be documented easily
Tcl UserWare API	Allows interfacing with tool flow and definition of rule checks

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