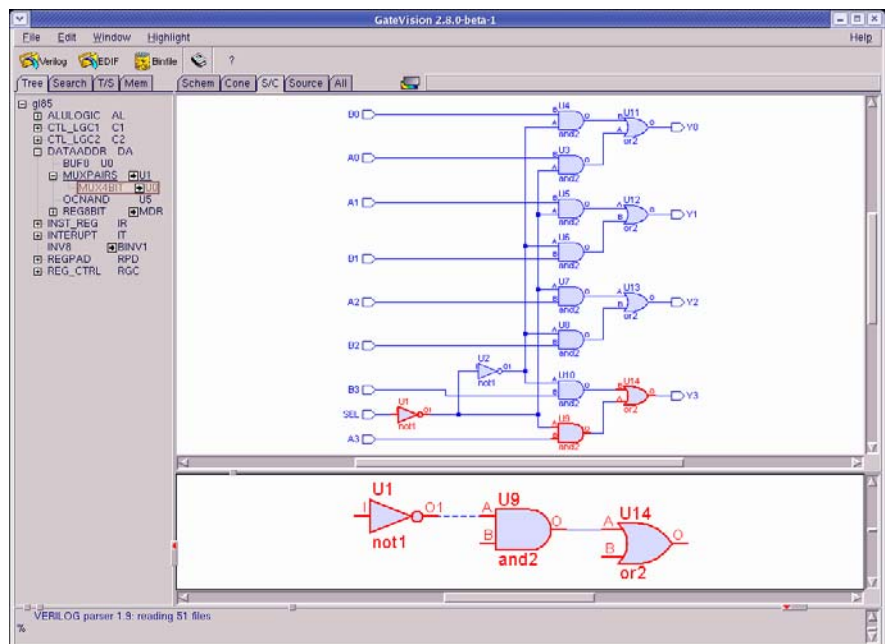


GateVision[®] PRO: New Power for Gate-Level Debugging

GateVision PRO is the third generation of graphical netlist analyzers from Concept Engineering. Completely rewritten to run on 32/64bit platforms, GateVision PRO provides the designer of even the largest chips with intuitive design navigation, schematic viewing, logic cone extraction and interactive logic cone viewing for debug support and design documentation.

Using Verilog or EDIF netlists, GateVision PRO fits seamlessly into any design environment. The power of the underlying algorithms allows schematics to be created on the fly and the intuitive GUI lets the designer search for critical paths, for paths between specific components or for specific areas in the design. These can be bookmarked for future use, or cross-probed between different design views. Critical path fragments can be exported as Verilog netlists for critical path simulation.



- Graphical netlist analyzer – Verilog or EDIF netlists
- Tcl based UserWare API – for advanced customization
- 32/64 bit database handles today's largest SoCs, ASICs and FPGAs
- Intuitive GUI for ease of use
- Customizable path extraction engine finds critical paths
- Cone view extracts schematic fragments of critical areas
- Cookie cutting – Verilog fragments can be saved as separate files

API – a tcl based UserWare API provides full access to the new 32/64-bit based database, for highly flexible customization. The designer can extend the functionality of GateVision PRO, adding, for example, electrical rule checking (ERC), report and documentation functions. The API also allows GateVision PRO to be closely integrated with different design flows and third party tools.

32/64 Bit – exploiting the increasing powerful 64 bit platforms, such as XEON®, Opteron™, UltraSPARC®, POWER™ and Itanium®, GateVision PRO runs quickly and efficiently, even for the largest and most complex of today's demanding ASICs, SoCs and FPGAs. The underlying database has been completely redesigned for efficient 64-bit operation.

Logic cone – the GateVision PRO logic cone provides interactive navigation within a schematic fragment, that portion of the circuit that is most relevant. This can be extended and reduced for signal path tracing through the complete design hierarchy.

Path extraction – the customizable path extraction engine can automatically identify and extract critical paths in a design. These can be explored and cross-probed in different views to reduce both the complexity and time of the debug cycle. A complete set of built-in path extraction capabilities includes input path extraction, output path extraction, and powerful user-configurable path extraction. Path fragments can be exported as Verilog netlists for critical path simulation.

GUI – the intuitive GUI provides a host of facilities including context sensitive menus and multiple views. A powerful search tool provides quick access to any object or group of objects in a design, with the results stored in a result list. Listed objects can be highlighted or moved into the logic cone window.

Views – built into GateVision Pro are a variety of view options, including schematic view, schematic fraction view, source code view, hierarchy tree view and object search view. Through these, and through cross-probing between views, it is possible to gain a deeper understanding of the device being debugged and to improve the debugging process.

At a Glance

FEATURE	BENEFITS
32/64 bit platform and on-the-fly schematic creation	Produces very high speed and capacity
UserWare API	Easily add custom capabilities for increased productivity
Automatic path extraction	Automatically extracts logic cones from user-defined reference points, and shows only the relevant portion of the circuit, Reduces complexity in the design for improved and faster debug
Verilog and EDIF netlist interface	Easily plugs into almost any design flow
Search-and-show capability	Easy location of specific objects shortens debug time
Design hierarchy browser	Provides easy navigation through the design hierarchy and gives compact hierarchy overview
Object cross-probing	Highlights selected objects in all design views (schematic, logic cone and HDL view) and shortens debug time
Context-sensitive menus	Easy-to-use GUI

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